PCMCIA 2.1 Compliant Low Power SRAM Memory Cards 512 K through 2 Megabyte Cards with Rechargeable Battery and Isolated Control Line Circuit Feature

Description

These products are high quality PCMCIA 2.1 compliant, 512KByte through 2MByte SRAM memory cards which operate in a 5.0 Volt only environment. SRAM technology is backed up by a rechargeable lithium battery, which assures long life data retention, even when system power is removed.

These cards feature a fully buffered interface to ensure excellent signal integrity. Control signals are also isolated from the Host socket and forced to an inactive state when the card is removed from the socket. In addition data may be handled in either 8 bit or 16 bit bus modes.

Features

- PCMCIA 2.1 compliant
- Single 5.0 Volt Power Supply
- Standard SRAM Read/Write Timing
- Standard 150 ns Access Time from Standby
- Byte-wide and Word-wide access
- Dedicated Attribute Memory EE PROM
- TTL compatible inputs and outputs
- Buffered I/O Address and Data lines
- Isolated Control Lines
- Secure Data Storage
  - ♦ Rechargeable battery back-up
  - ♦ Long Battery Charge Retention up to 18 months
- Low Power Consumption*
  - ♦ 100⌠A Max. Standby Current
  - ♦ 20mA Max. Operating Current (CMOS)
  - ♦ 70mA Max. Operating Current (TTL)
- ISO 9001 Quality Controls

* *Values indicated for Card while not executing Battery Recharge Cycle.*

PIN DESCRIPTION

Signal	Name	Function
A[25:0]	Address Bus	Address Inputs, A25-A0
D[15:0]	Data Bus	Data Input/Outputs
/OE	Output Enable	Active Low for Read
/WE	Write Enable	Active Low for Write
/CE1	Card Enable Low Byte	Active Low for Read/ Write Even Byte
/CE2	Card Enable High Byte	Active Low for Read/ Write Odd Byte
/REG	Register Select	Active Low enables Attribute Memory
WP	Write Protect	Output Signal indicates the WP switch state
$/BVD_1$,$/BVD_2$	Battery Voltage Detects	Indicate to the Battery Status
$/CD_1$,$/CD_2$	Card Detects	Tied to GND
V_{CC}	Power Supply	Power Supply Voltage, 5.0V ±5%
GND (V_{SS})	Ground	System Ground

PIN ASSIGNMENTS

Pin #	Signal	I/O	Function	State	Pin #	Signal	I/O	Function	State
1	GND		Ground		35	GND		Ground	
2	D3	I/O	Data Bit 3	PL	36	/CD1	O	Card Detect - Grounded	
3	D4	I/O	Data Bit 4	PL	37	D11	I/O	Data Bit 11	PL
4	D5	I/O	Data Bit 5	PL	38	D12	I/O	Data Bit 12	PL
5	D6	I/O	Data Bit 6	PL	39	D13	I/O	Data Bit 13	PL
6	D7	I/O	Data Bit 7	PL	40	D14	I/O	Data Bit 14	PL
7	/CE1	I	Card Enable Low byte	PH	41	D15	I/O	Data Bit 15	PL
8	A10	I	Address Bit 10		42	/CE2	I	Card Enable High byte	PH
9	/OE	I	Output Enable	PH	43	/VS1		Vltg Sense Signal 1- Open	
10	A11	I	Address Bit 11		44	*RFU*		*Reserved For Future Use*	NC
11	A9	I	Address Bit 9		45	*RFU*		*Reserved For Future Use*	NC
12	A8	I	Address Bit 8		46	A17	I	Address Bit 17	
13	A13	I	Address Bit 13		47	A18	I	Address Bit 18 **(Note 1)**	
14	A14	I	Address Bit 14		48	A19	I	Address Bit 19 **(Note 2)**	PL
15	/WE	I	Write Enable	PH	49	A20	I	Address Bit 20 **(Note 3)**	PL
16	/BUSY	O	Ready Busy Signal	NC	50	A21	I	Address Bit 21 **(Note 4)**	PL
17	V_{CC}		Power Supply		51	V_{CC}		Power Supply	
18	*Vpp1*		*Program Voltage 1*		52	*Vpp2*		*Program Voltage 2*	
19	A16	I	Address Bit 16		53	A22	I	Address Bit 22 **(Note 5)**	PL
20	A15	I	Address Bit 15		54	A23	I	Address Bit 23	NC
21	A12	I	Address Bit 12		55	A24	I	Address Bit 24	NC
22	A7	I	Address Bit 7		56	A25	I	Address Bit 25	NC
23	A6	I	Address Bit 6		57	/VS2		Vltg Sense Signal 2- Open	
24	A5	I	Address Bit 5		58	RESET	I	Hardware RESET	NC
25	A4	I	Address Bit 4		59	WAIT	O	Wait State Control **(Note 6)**	NC
26	A3	I	Address Bit 3		60	*RFU*		*Reserved For Future Use*	NC
27	A2	I	Address Bit 2		61	/REG	I	Register Select	PH
28	A1	I	Address Bit 1		62	/BVD2	O	Batt. Voltage Detect 2	PH
29	A0	I	Address Bit 0	PL	63	/BVD1	O	Batt. Voltage Detect 1	PH
30	D0	I/O	Data Bit 0	PL	64	D8	I/O	Data Bit 8	PL
31	D1	I/O	Data Bit 1	PL	65	D9	I/O	Data Bit 9	PL
32	D2	I/O	Data Bit 2	PL	66	D10	I/O	Data Bit 10	PL
33	WP	O	Write Protect		67	/CD2	O	Card Detect - Grounded	
34	GND		Ground		68	GND		Ground	

Notes :

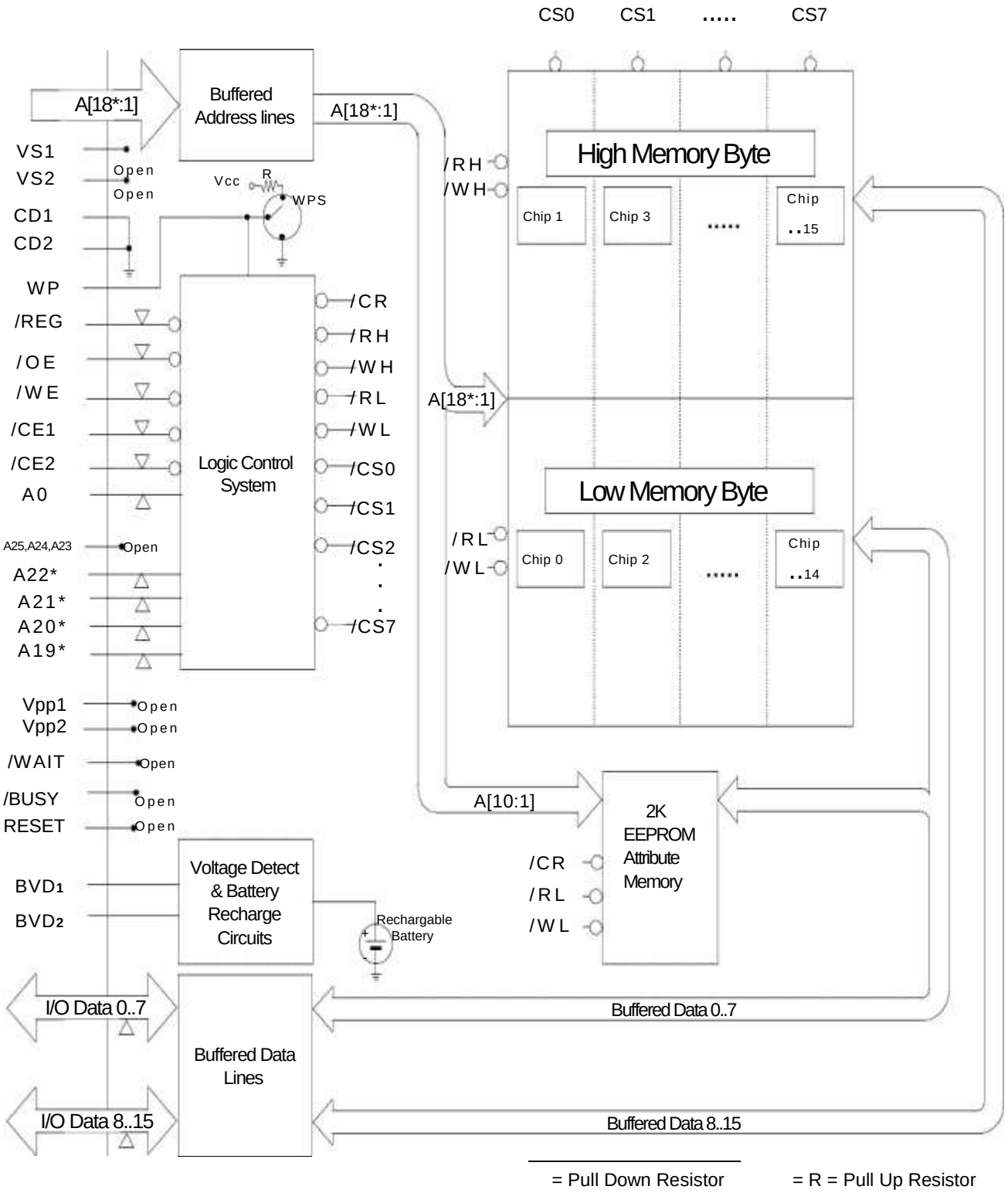
1. *Not Connected for cards of 256 Kilobyte capacity or lower. This signal is buffered for cards with the 4 Mbit component and pulled up for cards using the 1 Mbit component. Refer to the Product Description for memory component size.*
2. *Not Connected for cards of 512 Kilobyte capacity or lower.*
3. *Not Connected for cards of 1 Megabyte capacity or lower.*
4. *Not Connected for cards of 2 Megabyte capacity or lower.*
5. *There are no wait states generated by these cards. This signal must be pulled high by the Host socket.*

Legend :

I = *Input to card only*
O = *Output from card only*
I/O = *Bi-directional signal PH =Pulled High (10 - 50K Typ.) PL =Pulled Low (100K Min.) NC = Not Connected*

Functions of the shaded pins are not used.

FUNCTIONAL BLOCK DIAGRAM



*** Refer to Pin Assignment Section for address line No Connects.**

Note: **Block diagram is for fully populated card, component population is dependent on card configuration.**

COMMON MEMORY BUS OPERATIONS

Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ								
Read Even (x8)	H	H	L	L	H	L	High -Z	**Data Out-Even**
Read Odd (x8) **(Note 1)**	H	H	L	L	H	H	High -Z	**Data Out-Odd**
Read Odd (x8)	H	L	H	L	H	X	**Data Out-Odd**	High-Z
Read Word (x16)	H	L	L	L	H	X	**Data Out-Odd**	**Data Out-Even**
WRITE/ERASE								
Write Even (x8)	H	H	L	H	L	L	High -Z	**Data In-Even**
Write Odd (x8) **(Note 1)**	H	H	L	H	L	H	High -Z	**Data In-Odd**
Write Odd (x8)	H	L	H	H	L	X	**Data In-Odd**	High-Z
Write Word(x16) **(Note 2)**	H	L	L	H	L	X	**Data In-Odd**	**Data In-Even**
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Notes:

1. *Byte access - Odd. In this x8 mode, A0 = V_{IH} outputs or inputs the "odd" byte (high byte of the x16 word on D0 - D7). This is accomplished internal to the card by transposing D8-D15 to D0-D7.*
2. *During 16-bit write and erase operations one IC of a device pair may complete the operation prior to the other. It is therefore necessary to poll both components before considering the operation complete.*

Legend:

H = V_{IH}
L = V_{IL}
X = Don't Care

Warning: Raising address lines to voltage levels above a CMOS level is not permitted. Applying voltages above these levels will destroy the card. Any attempt to identify memory components in this way is not permitted.

ATTRIBUTE MEMORY BUS OPERATIONS

Pins/Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ (Note 1)								
Read Even (x8)	L	H	L	L	H	L	High -Z	**Data Out-Even**
Read Odd (x8) **(Note 2)**	L	H	L	L	H	H	High -Z	Data Out-Odd Not Valid
Read Odd (x8) **(Note 2)**	L	L	H	L	H	X	Data Out-Odd Not Valid	High-Z
Read Word (x16) **(Note 2)**	L	L	L	L	H	X	Data Out-Odd Not Valid	**Data Out-Even**
WRITE (Note 1)								
Write Even (x8)	L	H	L	H	L	L	High -Z	**Data In-Even**
Write Odd (x8) **(Note 3)**	L	H	L	H	L	H	High -Z	Data In-Odd Not Valid
Write Odd (x8) **(Note 3)**	L	L	H	H	L	X	Data In-Odd Not Valid	High-Z
Write Word (x16) **(Note 3)**	L	L	L	H	L	X	Data In-Odd Not Valid	**Data In-Even**
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Note:

1. *Refer to the data sheets for the Microchip 28C16A EEPROM for details on programming the attribute memory.*
2. *Data Read operations will produce data information that has no valid meaning for the Odd byte of information.*
3. *Data Write operations may be initiated, however data information for the Odd byte will not be stored.*

Legend:

H = V_{IH}
L = V_{IL}
X = Don't Care

Warning: Raising address lines to voltage levels above a CMOS level is not permitted. Applying voltages above these levels will destroy the card. Any attempt to identify memory components in this way is not permitted.

PIN DESCRIPTIONS

Vcc
Card Power Supply

Power input required for device operation. The Vcc must be 5.0 V ± 5% (4.75 V to 5.25 V).

GND
Card Ground

The V_{SS} pins of all IC components and related circuitry are connected to this card ground, which must be connected to the Host system's ground.

NC
Not Connected

These pins are physically not connected to any circuitry.

A0-A25
Address Bus

These signals are address input lines that are used for accesses to card memory. A0 is used to select the odd or even bank of memory components. A19 through A22 select which Device Pair of ICs will be accessed. A1 through A17 are used to select the specific address that is to be accessed on an individual memory component. A18 can be used to either select device pairs or to select a specific address on a memory component. Please refer to the Pinout Assignment Section for more detail. A23, A24 and A25 are not used and are Not Connected.

D0-D15
Data (Input/Output) Bus

Data lines D0 through D15 are used to transfer data to and from the card. When memory is not selected or outputs are disabled data lines are placed in a high impedance state.

/OE
Output Enable Signal

This active low input signal enables memory devices to activate data lines and output data information.

/WE
Write Enable Signal

This active low input signal controls memory write functions and is used to strobe data into the card memory.

WP
Write Protect Signal

This output signal indicates whether the Write Protect Switch (WPS) has disabled a card write operation. When the signal is asserted high, card write operations are disabled. When this signal is asserted low, card write operations function normally.

/CE1, /CE2
Card Enable

These are active low inputs used to enable the card memory. /CE1 accesses the low bank of memory, which provides storage for even numbered bytes. /CE2 accesses the high bank of memory, which provides storage for odd numbered bytes. During byte-wide operations these Card Enable signals are used in conjunction with address line A0 to access even or odd bytes of data. The memory card is de-selected and power consumption is reduced to stand-by levels when both /CE1 and /CE2 are driven high.

PIN DESCRIPTIONS *(CONTINUED)*

/REG
Register Select Signal

This active low input signal enables access to the Attribute memory EEPROM. Attribute memory is typically used to store the CIS file, which contains specific card information. Access to common memory is not possible when /REG is asserted low.

RESET
RESET Signal

This is an active high input signal that normally is used by the Host to place the card in the deep power down mode of operation. On these cards this signal is Not Connected.

/WAIT
Extended Bus Cycle

This active low output signal is used by the card to delay completion of a memory access operation. There are no wait states generated by these memory cards. For this reason the /WAIT signal is left open. It is the responsibility of the Host to pull this signal high to prevent false activation.

/BUSY
Ready Busy Signal

This active low output signal normally indicates that at least one memory device in the card is busy performing a task. On these cards this signal is Not Connected.

/CD1, /CD2
Card Detect

These pins are tied directly to ground and are used by the Host system to detect the presence of the card. If /CD1 and /CD2 are not both detected low by the Host, then the card is not properly inserted.

/VS1, /VS2
Voltage Sense Signals

The Voltage Sense Signals notify the socket of the card's Vcc requirements on initial power up. When both /VS1 and /VS2 are open, as is the case on these cards, the card is identified to the Host system as a 5V only card.

/Vpp1, /Vpp2
Program and Peripheral Voltages

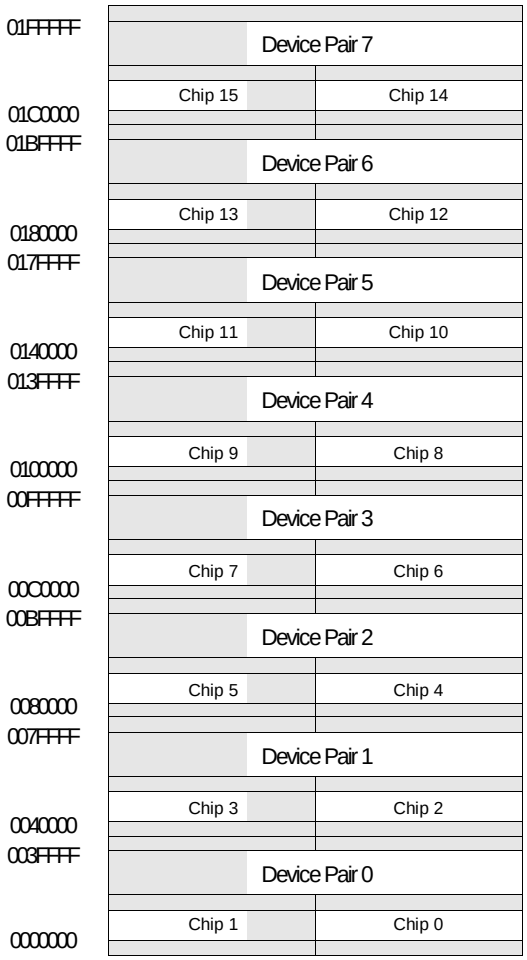
These signals are used to supply additional programming voltages for memory devices that require programming voltages other than the Vcc supply. These memory cards require only Vcc voltages, therefore Vpp1 and Vpp2 are Not Connected.

/BVD1, /BVD2
Battery Voltage Detect

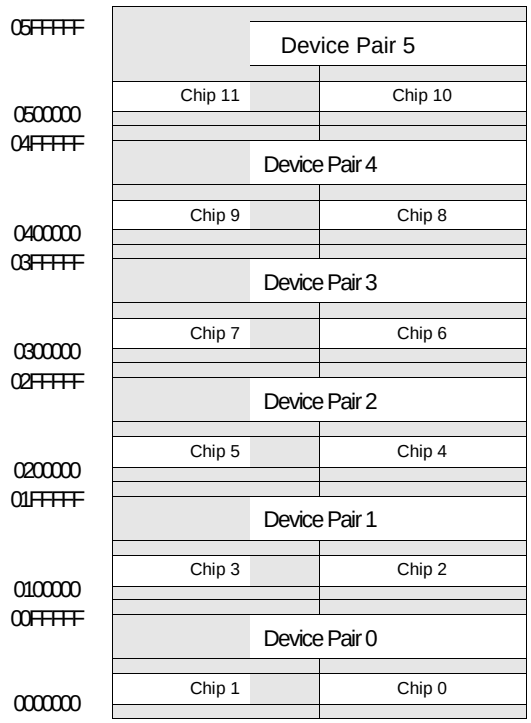
These pins are normally used to indicate the status of an internal card battery. When both signals are in a high state the stored data is sufficient to guarantee data retention. When /BVD2 is in a low state and /BVD1 is in a high state the stored data is retained, however the battery should be recharged. If both signals are in a low state any stored data will have been lost and the batter will need to be recharged be for the card can be used to store data again.

CARD COMMON MEMORY MAP

For Cards Using 1Mbit Components*



For Cards Using 4Mbit Components*



*These device maps are depicting full capacity cards, actual device population is dependent on card capacity.

CARD TIMING CHARACTERISTICS

(Standard operating times for both Common and Attribute Memory unless otherwise noted.) **Read Cycle Timing (/WE = V_{HI})**

Parameter	Symbol	Min	Max	Units
Read Cycle Time	t_{AVAV}	150		ns
Address Access Time	t_{AVQV}		150	ns
Card Enable Access Time	t_{ELQV}		150	ns
Output Enable Access Time	t_{GLQV}	100		ns
/OE High to Data Output Disable	t_{GHQZ}		75	ns
/CE Low to Data Output Enable	t_{ELQNZ}	5		ns
Address change to Data no longer valid	t_{AXQX}	0		ns
Address Setup to /OE Low time	t_{AVGL}	20		ns
/OE High Setup to Address time	t_{GHAX}	20		ns
/CE Low Setup to /OE Low time	t_{ELGL}	0		ns
/OE High to /CE High Hold time	t_{GHEH}	20		ns

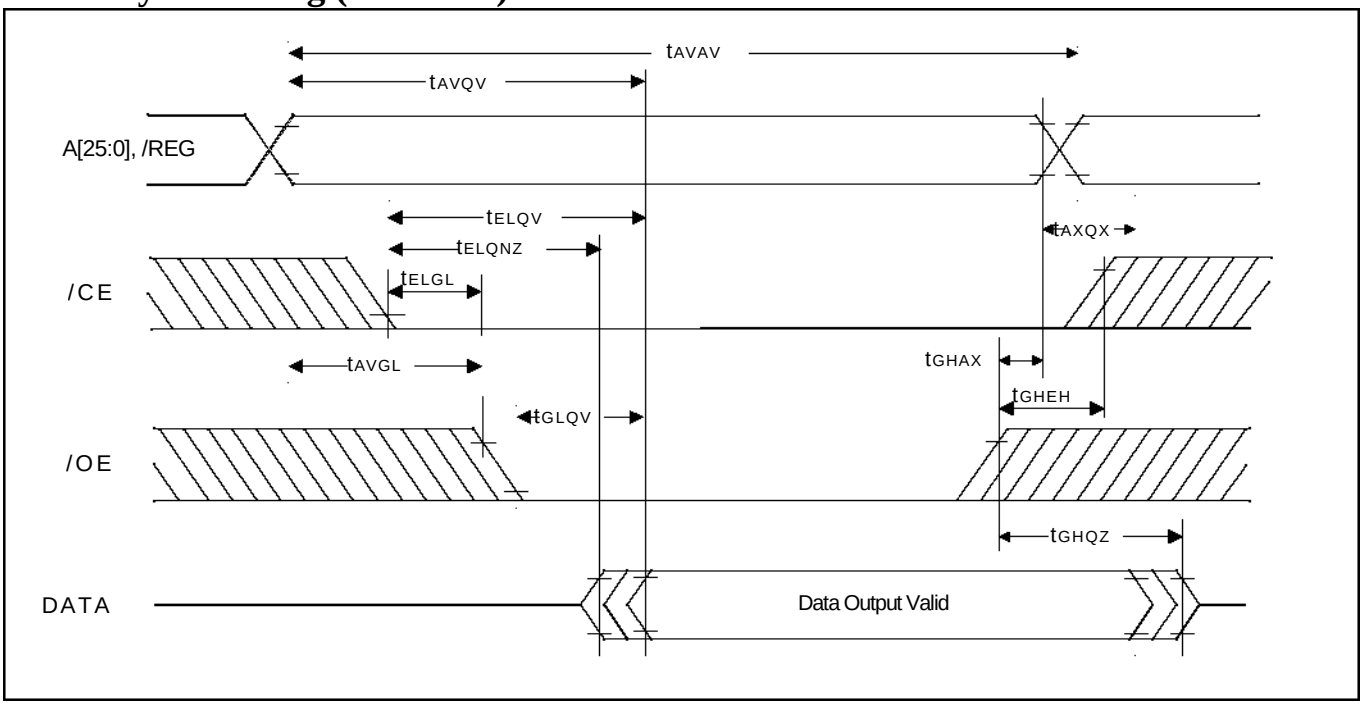
Write Cycle Timing (/OE = V_{HI})

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{AVAV}	150		ns
Write Pulse Width	t_{WLWH}	80		ns
Address Setup Time for /WE Low	t_{AVWL}	20		ns
Address Setup to /WE High	t_{AVWH}		100	ns
Card Enable Setup to /WE Low	t_{ELWH}	100		ns
Data Setup to /WE High	t_{DVWH}	50		ns
Data Hold from /WE High	t_{WHDX}	20		ns
Address Hold from /WE High	t_{WHAX}	20		ns
Data Output Disable Time form /WE Low	t_{WLQZ}		75	ns
Data Output Disable Time form /OE Low	t_{GHQZ}		75	ns
/WE High time to Data Output Enable	t_{WHQNZ}	5		ns
/OE Low time to Data Output Enable	t_{GLQNZ}	5		ns
/OE High to /WE Low Setup time	t_{GHWL}	10		ns
/WE High to /OE Low Hold time	t_{WHGL}	10		ns
/CE Low to /WE Low Setup time	t_{ELWL}	0		ns
/WE High to /CE High Hold time	t_{WHEH}	20		ns

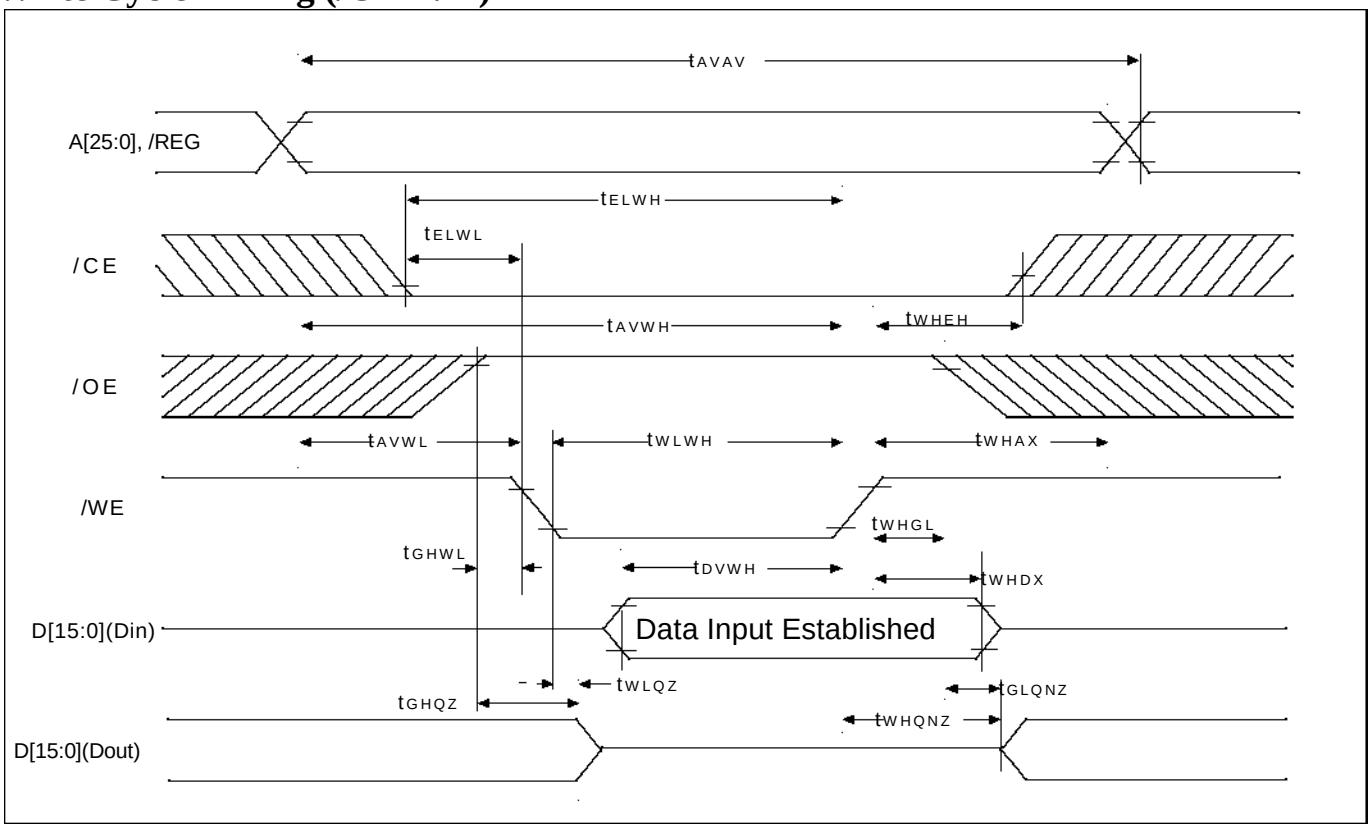
CARD TIMING CHARACTERISTICS *(CONTINUED)*

Common and Attribute Memory Read and Write Cycle Timing.

READ Cycle Timing (/WE=V_{IH})



Write Cycle Timing (/OE=V_{IH})



RECOMMENDED DC OPERATING CONDITIONS

Parameter	SL Version	SR Version	SI Version
Operating Temperature	0°C - 60°C	0°C - 60°C	-20°C - 60°C
Storage Temperature	-40°C - 80°C	-40°C - 80°C	-40°C - 80°C

Parameter Symbol	Parameter Description	Minimum	Typical	Maximum	Unit
V_{CC}	Supply Voltage	4.75	-	5.25	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Note 1)	2.0	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Minimum	Maximum	Unit
I_{LI1}	Input Leakage Current (Note 1)	V_{IN} = V_{CC} or GND	-10	10	uA
I_{LI2}	Input Leakage Current (Note 2)	V_{IN} = V_{LH}	-	0.5	mA
I_{LI3}	Input Leakage Current (Note 3)	V_{IN} = V_{LL} or GND	-	0.05	mA
I_{LO}	Output Leakage Current (Note 3)	V_{CC} = V_{CC} Max, V_{OUT} = V_{CC} or V_{SS}	-10	10	uA
I_{CC1}	Average Operating Current 1 (CMOS) (Note 4)	Cylcle Time 1∫s, 100%Duty /CE δ 0.2V, V_{IH} ε V_{CC} - 0.2V V_{IL} ε 0.2V, I_{OUT} = 0mA	-	20	mA
I_{CC2}	Average Operating Current 2 (TTL) (Note 4)	Cylcle Time 1∫s, 100%Duty /CE = V_{IL} V_{in} = V_{IL} or $_{VIH}$, I_{OUT} = 0mA	-	70	mA
I_{CCS}	V_{CC} Standby Current (CMOS) (Note 5)	/CE ε V_{CC} - 0.2 V V_{in} ε V_{CC} - 0.2V or V_{in} δ 0.2V	-	100	uA
V_{OH}	Output High Voltage	I_{HO} = -1.0 mA	2.4	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA	-	0.4	V
I_{PU}	Pull up current	V_{in} = 0V, V_{CC} = 5V		0.5	mA
I_{PD}	Pull down current	V_{in} = V_{CC} = 5V		0.05	mA

Notes:

1. *Values specified are per interface pin not connected to either a pull up or pull down resistor network.*
2. *Value specified is per interface pin connected to a 10KΣ~ pull up circuitry.*
3. *Value specified is per interface pin not connected to 100KΣ~ pull down circuitry.*
4. *Value indicated is per active Byte (8 bits) of information accessed form either High or Low memory.*
5. *Value indicated for a card with a fully charged internal battery. If the internal battery is insufficiently charged, the battery recharge cycle will be initiated, causing additional current to be drawn from the host during that cycle. (See Battery Charge and Data Retention)*

POWER SUPPLY SEQUENCE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max	Units
Detection Rising Voltage	Vinh	4.2	4.3	4.4	V
Detection Falling Voltage	Vinl	4.1	4.2	4.3	V
CE Setup Time	tsu(CE)			10	ms
Protection Time	tp(CE)	0.5			ms
Battery Backup Setup Time	tbs	10			⌠s
/CE Recovery Time	trec	100			ns

BATTERY CHARGE AND DATA RETENTION

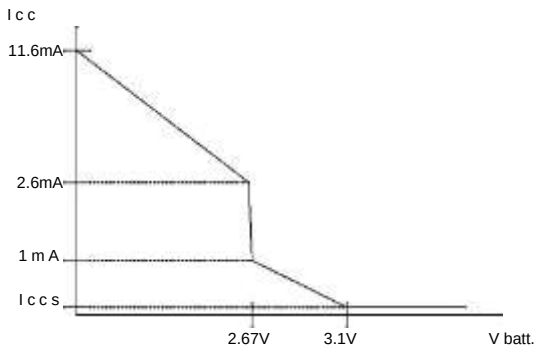
The rechargeable battery installed in this product will typically hold its charge for a period shown in the chart below for the different products. This value, however, is not intended to be used as a mark for calculating valid data retention shelf life. It is also important to note that changes in the ambient temperature will shorten the battery charge hold time. Maintaining a charge on the battery ensures that data is safely retained. The BVD_1 and BVD_2 pins indicate the status of the battery charge (See Table below) and the on board battery recharge circuitry initiates a recharge cycle when required.

Current Draw verse Battery Voltage

BVD2	BVD1	Battery Status
H	H	Battery voltage is guaranteed to retain data
L	H	Data valid, battery should be recharged
L	L	Data no longer valid, battery must be recharged.

Data Retention (at 20°C)

Min 12 months



CARD INFORMATION STRUCTURE

The CIS is data that describes the PCMCIA card and is described by the PCMCIA standard. This information can be used by the Host system to determine a number of things about the card that has been inserted. For information regarding the exact nature of this data, and how to design Host software to interpret it, refer to the PCMCIA standard Metaformat Specification.

Physical Address	Logical Address	Data Value(s)	Tuple Description
00h	00h	01h	CISTPL_DEVICE
02h	01h	03h	CISTPL_LINK
04h	02h	53h	Speed = 150ns, WPS=Yes, FLASH
06h	03h	**0Eh** ***(Note 1)***	Bits 2-0 = 110b = 2 Meg units, Bits 7-3 = 00001b = 2 Units (0=1, 1=2...) 2 Meg x 2 = 4 Meg size
08h	04h	FFh	CISTPL_END - End of Tuple

0Ah	05h	1Eh	CISTPL_DEVICEGEO
0Ch	06h	07h	CISTPL_LINK
0Eh	07h	02h	DGTPL_BUS - Bus Width - 2 Bytes
10h	08h	11h	DGTPL_EBS - Erase Block Size 2^10h = 64K Bytes or Words
12h	09h	01h	DGTPL_RBS - Byte Accessible
14h	0Ah	01h	DGTPL_WBS - Byte Accessible
16h	0Bh	01h	DGTPL_PART - One Partition
18h	0Ch	01h	DGTPL_HWIL - No Interleave
1Ah	0Dh	FFh	CISTPL_END - End of Tuple

Note:

1. *Refer to the table (right) for Part numbers, card memory capacity and corresponding data value.*

Part Number	**Memory Capacity**	**Data value**
VTR-SRA-512	512 Kilobyte	1C
VTR-SRA-001	1 Megabyte	3C
VTR-SRA-002	2 Megabyte	0C

Continued next page.

CARD INFORMATION STRUCTURE *(CONTINUED)*

Physical Address	Logical Address	Data Value(s)	Tuple Description
1Ch	0Eh	15h	CISTPL_VERS1
1Eh	0Fh	72h	CISTPL_LINK
20h	10h	04h	TPLLV1_MAJOR (PCMCIA 1.1/JEIDA 4.2)
22h	11h	01h	TPLLV1_MINOR
24h...5Ch	12h...2Eh	43 65 6E 74 65 6E 6E 69 61 6C 20 54 65 63 68 6E 6F 6C 6F 67 69 65 73 2C 20 49 6E 63 2E	
5Eh	2Fh	00	NULL String Delimiter (String 1)
60...7Ah	30h...3Dh	53 4C 30 34 4D 2D 31 35 2D 31 31 31 37 34	
7Ch	3Eh	00	NULL String Delimiter (String 2)
7Eh..FCh	3Fh...7Eh	32 20 4D 45 47 20 53 52 41 4D 20 77 2F 20 57 72 69 74 65 20 50 72 6F 74 65 63 74 20 2D 20 31 35 30 20 6E 73 52 65 63 68 61 72 67 65 61 62 6C 65 20 4C 69 74 68 69 75 6D 20 42 61 74 74 65 72 79	
FEh	7Fh	00	NULL String Delimiter (String 3)
100h	80h	00	NULL String Delimiter (String 4)
102h	81h	FF	CISTPL_END - End of Tuple
104h	82h	FF	CISTPL_END - End of Chain Tuple